Complete Listing of Claims:

1. (Currently amended) A method of adjusting carrier mobility for different semiconductor conductivities on the same chip comprising steps, in sequence, of:

~~provided~~ forming a first layer of material ~~providing~~ applying a first stress level on a portion of a surface of a chip,

selectively reducing said first stress level of a portion of said first layer of material,

~~providing~~ forming a second layer of material ~~providing~~ applying a second stress level on a portion of a surface of the chip said second stress level being different from said first stress level, and

selectively reducing said second stress level of a portion of said second layer of material.

2. (Currently amended) The method as recited in claim 1, wherein said first stress level is tensile and said second stress level is compressive.

3. (Original) The method as recited in claim 1, wherein said step of providing a first layer is performed by plasma enhanced chemical vapor deposition.

4. (Original) The method as recited in claim 3, wherein said first stress level is developed in accordance with plasma power during said plasma enhanced chemical vapor deposition.

5. (Original) The method as recited in claim 1, wherein said step of providing said second layer is performed by thermal chemical vapor deposition.

6. (Original) The method as recited in claim 5, wherein said step of providing a first layer is performed by plasma enhanced chemical vapor deposition.

7. (Original) The method as recited in claim 6, wherein said first stress level is developed in accordance with plasma power during said plasma enhanced chemical vapor deposition.

8. (Original) The method as recited in claim 1, wherein one of said first layer of material and said second layer of material is silicon nitride or silicon oxynitride.

9. (Currently amended) The method as recited in claim 1, including the further step of:

forming two transistors in said portion of a surface of a chip prior to said steps of providing said first and second layers of material.

10. (Original) The method as recited in claim 1, wherein said step of providing a second layer of material results in a greater thickness than a thickness resulting for said step of providing a first layer of material.

11. (Currently amended) The method as recited in claim 1, wherein said steps of reducing stress are performed by implanting ions of germanium, arsenic, xenon, indium, antimony, silicon, nitrogen, oxygen or carbon.

12. (Withdrawn) An integrated circuit comprising

a first circuit element,

a second circuit element,

a first layer of material overlying said first circuit element and said second circuit element and having a first stress level in a first region of said first layer and a second stress level in a second region of said first layer, and

a second layer of material overlying said first circuit element and said second circuit element and having a first stress level in a first region of said second layer and a second stress level in a second region of said second layer, wherein said second stress level in each of said first and second layers is reduced from the first stress level in each of said first and second layers.

13. (Withdrawn) The integrated circuit as recited in claim 12, wherein said first layer and said second layer comprise an etch stop layer.

14. (Withdrawn) The integrated circuit as recite in claim 12 wherein one of said first layer and said second layer is one of silicon nitride or silicon oxynitride.

15. (Withdrawn) The integrated circuit as recited in claim 12, wherein said first circuit element is a first transistor and said second circuit element is a second transistor.

16. (Withdrawn) The integrated circuit as recited in claim 15, wherein said first and second transistors are field effect transistors of complementary conductivity types.

17. (Withdrawn) The integrated circuit as recited in claim 12, wherein said second region of each of said first and second layers is implanted with a heavy ion.

18. (Withdrawn) The integrated circuit as recited in claim 17, wherein said heavy ions are of germanium, arsenic, xenon, indium, antimony, silicon, nitrogen oxygen or carbon.

19. (Withdrawn) The integrated circuit as recited in claim 12, wherein said first layer and said second layer are of different thickness.

20. (Withdrawn) The integrated circuit as recited in claim 12, wherein said first stress levels in each of said first and second layers is in the range of -2.0 to +2.0 GPa.